REMARKS

Claims 1-22 are pending in the present application. The following remarks relate to comments made in the Final Office Action sent prior to the present Request for Continued Examination.

Claims 3, 12, and 19 were rejected under 35 U.S.C. § 112, first paragraph, as allegedly failing to comply with the enablement requirement in that the phrase "the inserted zeroes comprise an equivalent time varying convolution code" is not described in the specification. Applicants respectfully disagree and note that the Patent Application describes a "zero code" comprising an equivalent time varying convolutional code at least in lines 1-5 on page 13 of the specification. The Examiner alleges that the specification does not specifically state "the inserted zeroes comprise an equivalent time varying convolution code" and therefore alleges that the specification does not enable claims 3, 12, in 19. Applicants respectfully submit that it is not necessary for the specification to use precisely the same terminology as used in the claims, as long as the written description enables a person of ordinary skill in the art to make and use the claimed invention. Applicants submit that the specification contains sufficient information regarding inserted zeroes that may comprise an equivalent time varying convolution code to enable a person of ordinary skill in the art to make and use the claimed invention. Applicants respectfully request that the Examiner's rejections of claims 3, 12, and 19 under 35 U.S.C. § 112, first paragraph, be withdrawn.

Claims 1-16 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by Kato, et al (U.S. Patent No. 5,436,918). Claims 17-22 were rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Kato in view of Wicker. The Examiner's rejections are respectfully traversed.

With regard to independent claims 1, 10, and 17, Applicants describe and claim, among other things, periodically inserting known symbols into a digital input data sequence based on a constraint length. By periodically inserting known symbols into the digital input data sequence based on a constraint length, the present invention may reduce the computational complexity of the channel coding system, may reduce the required memory storages, and may reduce the bit error rate. See Patent Application, page 7, ll. 16-25.

In contrast, Kato describes inserting fixed bits in a bit stream. The fixed bits may be inserted near the central portion of encoding information bit data. In the case of inserting a plurality of bits, the bits may be inserted concentratedly or distributively. See Kato, col. 4, ll. 7-16 and Figures 5A-B. Kato argues that inserting the fixed bits may result in a lower residual bit error ratio for the *same* line bit error ratio (emphasis added). See Kato, col. 2, ll. 58-61. However, Kato does not describe or suggest periodically inserting known symbols into a digital input data sequence based on a constraint length.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Kato and request that the Examiner's rejections of claims 1-16 under 35 U.S.C. 102(b) be withdrawn.

Applicants also respectfully submit that the pending claims are not obvious in view of the cited references, either alone or in combination. To establish a *prima facie* case of obviousness, the prior art reference (or references when combined) must teach or suggest all the claim limitations. *In re Royka*, 490 F.2d 981, 180 U.S.P.Q. 580 (CCPA 1974). As discussed above, Kato does not describe or suggest periodically inserting known symbols into a digital input data sequence based on a constraint length. The Examiner relies upon Wicker to teach producing a generator matrix having a constraint length. However, Wicker does not remedy the

aforementioned fundamental deficiency with the primary reference. In particular, Wicker is completely silent with regard to inserting known symbols into a digital input data sequence based on the constraint length.

The cited references also fail provide any suggestion or motivation to modify the prior art to arrive at Applicants claimed invention. To the contrary, Kato teaches away from the present invention. In particular, Kato teaches that fixed bits are inserted in a data stream to reduce a residual bit error ratio for the *same* line bit error ratio, whereas the present invention teaches periodically inserting known symbols based on the constraint length to *reduce* the line bit error ratio. It is by now well established that teaching away by the prior art constitutes *prima facie* evidence that the claimed invention is not obvious. *See, inter alia, In re Fine,* 5 U.S.P.Q.2d (BNA) 1596, 1599 (Fed. Cir. 1988); *In re Nielson*, 2 U.S.P.Q.2d (BNA) 1525, 1528 (Fed. Cir. 1987); *In re Hedges*, 228 U.S.P.Q. (BNA) 685, 687 (Fed. Cir. 1986).

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not obvious over Kato and Wicker, either alone or in combination. Applicants respectfully request that the Examiner's rejections of claims 17-22 under 35 U.S.C. 103(a) be withdrawn.

It is believed that no fee is due; however, should any fees under 37 C.F.R. §§ 1.16 to 1.21 be required for any reason, the Commissioner is authorized to deduct said fees from Williams, Morgan & Amerson's P.C. Deposit Account 50-0786/2100.005100.

The Examiner is invited to contact the undersigned at (713) 934-4052 with any questions, comments or suggestions relating to the referenced patent application.

Respectfully submitted,

Date: 5/4/05

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